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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,671	09/30/2004	Yao-Cheng Chiu	13693-US-PA	5670

31561 7590 06/28/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,671	CHIU, YAO-CHENG	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,10 and 12-16* is/are rejected.

7)☒ Claim(s) *4,5,9,11,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-8, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Chheda (Pub. No. US20040059859)

As per claims 1, 6, and 8, Chheda discloses a method for connecting low pin count (LPC, hereinafter) bus to serial flash memory, comprising: (a) fetching a LPC bus instruction; (paragraph 17 and 21, ie latching data or transaction in response to signal requests) (b) converting the LPC bus instruction to a serial instruction according to the required format of a serial flash memory(paragraph 22, ie converting data/address into compatible formatted); (c) provided the serial instruction is a write instruction, recording the serial instruction, accumulating write instructions until N instructions are received, combining the accumulated instructions and outputting to a serial flash memory at one time, where N is a preset positive integer(paragraph 16-27, ie implementing read/write transactions in a transaction module 201) ; (d) provided the serial instruction is a read instruction, reading M bytes of data from the serial flash memory and outputting

the data sequentially, where M is a preset positive integer(paragraph 16-27, ie serially drives the transactions from most significant to the lest significant onto the LPC bus in synchronization with the LPC clock); (e) converting an output data to the required format according to the LPC bus, where the output data is for responding to the LPC bus instruction; and (f) outputting the output data of converted format to the LPC bus. (paragraph 22, ie converting data/address into compatible formatted)

As per claims 2, 7, Chheda discloses the method further comprising: calculating a cycle count of a clock signal provided by the LPC bus instruction, for identifying a command field, an address field, and a data field of the serial instruction. (paragraph 26-28, ie implement transactions with LPC clock cycle)

As per claims 3,10, Chheda discloses wherein the procedure (c) comprises: recording the data field of the serial instruction and the data field of a plurality of former write instructions; and provided N data fields are accumulated and recorded, outputting the command field and the address field of the serial instruction to the serial flash memory, and outputting the recorded data field to the serial flash memory according to the sequence of recording. (paragraph 21-27)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12- 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chheda (Pub. No. US20040059859) in view of Messerly (US Patent 6,308,192)

As per claims 12-13, Chheda discloses an apparatus for connecting low pin count (LPC) bus and serial flash memory, comprising: a latch, for registering and outputting a LPC bus instruction transmitted from a LPC bus(paragraph 17 and 21, ie latching data or transaction in response to signal requests); an instruction converter, receiving the LPC bus instruction outputted from the latch, converting the LPC bus instruction to a serial instruction according to the required format of serial flash memory, and outputting the serial instruction(paragraph 22, ie converting data/address into compatible formatted); converter for receiving and recording the serial instruction outputted from the instruction converter, provided the serial instruction is a read instruction, accumulating and recording M read instructions, combining the read instructions, and converting the combined instruction for output, provided the serial instruction is a write instruction, accumulating and recording N write instructions, combining the write instructions, and converting the combined instruction for output, where M and N are both preset positive integer; a serial output device, for coupled in between the

converter and a serial flash memory, outputting the serial signals outputted from the parallel to serial converter to the serial flash memory; and converter, for receiving an output data which is needed for responding to the LPC bus instruction from the serial flash memory, converting the output data to the required format according to the LPC bus, and outputting the output data of converted format to the LPC bus. (paragraph 16-27, ie converting data/address into compatible formatted)

Chheda discloses all the limitations as above except a parallel to serial converter. However, Messerty discloses a synchronous parallel to serial device is provided to convert the parallel format of the output into a serial equivalent as a serial output signal and vice versa. (col.3, line 49-col.4, line 32)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Messerty's teaching into Chheda's system so as it would advance for fast processing times which suitable for high-speed applications and reduced numbers of filter elements. (col.2,lines 17-24)

As per claims 14, Chheda discloses the method further comprising: a counter, for receiving a clock signal provided by the LPC bus, calculating a cycle count of the clock signal, and outputting the cycle count to the parallel to serial converter and to the serial to parallel converter for identifying the command field, the address field, and the data field in the serial instruction.(paragraph 21-28)

As per claim 15, Chheda discloses a read register, when the serial instruction is a read instruction, for receiving M bytes of data from the serial flash memory at one time, converting the format of the data sequentially, and outputting to the LPC bus. (paragraph 21-28, ie implementing read/write transactions in a transaction module 201)

As per claim 16, Chheda discloses a batch read device, for receiving the command field and the address field of the serial instruction, and issuing instructions for reading M bytes of data from the serial flash memory at one time; a write register, provided the serial instruction is a write instruction, for receiving the data field of the serial instruction, storing the data field of the serial instruction and the data field of former N-1 write instructions, and outputting the data fields according to the sequence of stores; and a batch write device, for receiving the output data field from the write register, and receiving the command field and the address field of the serial instruction, provided the serial instruction is a write instruction, outputting the command field and the address field of the serial instruction as well as the data fields to the serial flash memory. (paragraph 21-28)

Allowable Subject Matter

5. Claims 4-5, 9, 11, 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's claimed invention is deemed allowable over the prior art of record as the prior art fails to teach or suggest wherein M/N is a preferred setting equivalent to the efficient size of a central processing unit (CPU, hereinafter) process divided by 8 in combination with other limitations as recited in independent claims and further in view of the specification and applicant's arguments.

Conclusion

6. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

June 21, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
6/23/06